PAD Interface Control Document (ICD)

Issue/Version	Date	Author	Details
1	circa 2007	Unknown	First Release
1B	15th August 2012	Peter Hayward	Updated to reflect operation with version 2.47 of the firmware
2	16th April 2013	Andrew Pauza	Tidy up versioning, formatting and naming. Add note: works with LNS software v4.7 (and higher) and FPGA v3.5. Added info on RF wait times as it is important though not actually part of the interface. Corrected register 9, bits 12-15 errors. Indicated point in Worked Command Sequence where and RF wait should occur.

1 Introduction

This document specifies the communications and control protocol for PCs interfacing the current generation of Owlstone's FAIMS hardware platform called "PAD" and herein referred to as "Sensor Sub-system".

Software/Firmware used	Version/Revision
Lonestar software	4.7
FPGA	3.5
PIC-USB	2.47
PC	WinXP-SP3, Win7 (32,64bit)

2 USB Communication : Sensor Sub-System <> Local PC

The USB stack on the Sensor Sub-System is implemented in a way that allows a virtual communication port to be installed on an interfaced PC. This virtual communications port is accessed in the same way that the RS232 ports are used. By emulating a serial link, a simple text based protocol is implemented to allow messages to be passed between the embedded PC and embedded processor.

The local PC accesses the virtual COM port and issues text strings formatted as command messages. These command messages are described in the **Command Messages** section (Section 2.1). Response messages are sent from the embedded processor to the local PC as formatted text strings. These response messages are described in the **Data Messages** section (Section 2.2).

To enable the pseudo-serial communications over the USB port a communications driver must be installed on the embedded PC. The information (.inf) and driver setup files specific to this product can be obtained from Owlstone. The PIC-USB Serial Driver is compatible with at least Windows XP Pro SP3 and Windows 7 (both 32 and 64 bit versions) – see Appendix 3.3

The hardware interface is defined as RS232 protocol at 115,200 baud with 8 data bits, 1 stop bit, no parity and no handshaking.

2.1 Command Messages

The Sensor Sub-System is controlled by setting registers in an FPGA (via the embedded processor) that subsequently control the various drive signals. The commands are given by single lower case characters. If the command takes a numeric argument the second character on the line must be a comma. Commands are terminated by an ASCII carriage return. All other ASCII control characters are ignored. There are a total of 42 registers on the FPGA. However not all of these are used for control. Only the registers involved in control are documented in this section.

2.1.1 Writing a command to an FPGA register

Format: use the ASCII "w" character, followed by the comma delimited value of the register address and the value to write. Values should be entered as optionally signed **ASCII character written decimal numbers**. Terminate the string using a carriage return:-

w,<address>,<value><CR>

if the command is successful the embedded processor will respond with the acknowledgement string

ok<CR>

If there is a problem, e.g. illegal register, malformed number etc then there will be a response of the form

error [optional text] <CR>

2.1.2 Reading back an FPGA Register Command

Format: use the ASCII "r" character, followed by a comma and then the register address. Terminate the string using a carriage return: -

r,<address><CR>

the embedded processor will respond with a FPGA register data message (see "Data Messages" Section). Values will be returned as **unsigned ASCII character written decimal numbers**. The returned value will always be unsigned, even if the register is defined as signed and written using a negative value.

2.1.3 Data Collection Command

Format: use the ASCII command 'g'. Terminate the string using a carriage return.

g<CR>

The embedded processor will respond with the acknowledgement string

ok<CR>

Notes

1) Data is collected in an internal buffer in the FPGA. The data in this buffer can optionally be returned to the user via the 'd' command.

2) The settings stored in FPGA_registers are only manifest as voltages while the system is running. This occurs following the issue of the 'g' command. To run the system continuously without collecting data the "g" command must be reissued whenever bit zero of register 9 is cleared. This marks the end of the sweep.

2.1.4 Read Acquired Data Message

Format: use the ASCII character "d". Terminate the string using a carriage return. The number of words returned is twice the value in the FPGA register 15 (the number of steps in the Compensation Voltage). The returned data is formatted as **ASCII hexadecimal words**.

d<CR>

the embedded processor will respond with an acquired data message (see "Data Messages Section")

2.2 Data Messages

2.2.1 FPGA Register Data Message

Format: a text string, starting with ASCII string 'fpga' followed by comma delimited list of the address and register parameters. Values will be returned as unsigned ASCII character written decimal numbers. A carriage return indicates message termination.

fpga,<address>,<value><CR>

2.2.2 Acquired Data Message

Format: a text string, starting with the ASCII string 'data' followed by a comma delimited list of hexadecimal formatted words, where a word is two bytes long. A carriage return indicates message termination. The number of words returned is determined by the value in FPGA register 15 (number of steps in the "Compensation Voltage") and will be **TWICE** this value.

data,<first word>,<second word>,...,<last word><CR>

e.g. data,AB01,AB02,AB03...*etc*

Where, for example, AB01 in hex is equivalent to 43777 in decimal. The data range will be integer values of 0 to 65535 corresponding to an Ion Current of –10 to +10 A.U.

2.3 Control Register Descriptions

The following lists each register on the FPGA embedded in Sensor Sub-System that serves to control output parameters. Note some register are read/write whilst some are read only. Registers are characterised by their size, function, range, default (setting when unit is first powered up) and format (as the decimal equivalent of the least significant bit). Read/write addresses also have a standard setting noted.

2.3.1 Address: 0 Read Only

Size: 16 bit

Function: FPGA firmware version.

Normal setting: 1035

2.3.2 Address: 1 Read/Write

Size: 12 bit signed

Function: Sensor temperature

Range: -2048 to + 2047 (-2048 to +2047 corresponds to -128 to +128℃)

Default setting: N/A

Format: 0.0625℃ per LSB

2.3.3 Address: 2 Read/Write

Size: 12 bit signed

Function: Set sensor temperature

Range: -2048 to + 2047 (-2048 to +2047 corresponds to -128 to +128℃)

Default setting: 0

Format: 0.0625℃ per LSB

Standard Setting: Heater on: w,2,800<CR> (sets temperature at 50℃)

Heater ambient (off): w,2,400<CR> (sets heater to 25℃)

2.3.4 Address: 3 Read/Write

Size: 12 bit signed

Function: Interface Board temperature sensor

Range: -2048 to + 2047 (-2048 to +2047 corresponds to -128 to +128℃)

Default setting: N/A

Format: 0.0625 ℃ per LSB

2.3.5 Address: 10 Read/Write

Size: 16 bit unsigned

Function: Sets the dispersion field pulse height

Range: 0 – 65535 (representing 0 to ~100.823% Full Scale Dispersion Field)

Default setting: 0

Format: 1.538461538 x 10^{-3} % full scale per LSB

Standard Setting: Varied step-wise in SW to build up dispersion field sweep data

2.3.6 Address: 13 Read/Write

Size: 16 bit signed

Function: Sets the start voltage of the Compensation Voltage sweep

Range: -16384 – +16384 (representing -50V to +50V)

Default setting: 0 (0V)

Format: 3.0517578125mV per LSB

Standard Setting: -2621 (-8.0V)

2.3.7 Address: 14 Read/Write

Size: 16 bit unsigned

Function: Sets the Compensation Voltage step size whole part

Range: 0 – 65535

Default setting: 0

Format: 3.0517578125mV step size per LSB

Standard Setting: Depends on step size user requires in CV dimension

Note: See also register 44, Compensation Voltage step size fractional part

2.3.8 Address: 15 Read/Write

Size: 13 bit unsigned

Function: Sets the number of steps in the Compensation Voltage. The number of A2D conversions is twice this value.

Range: 0 – 4096

Default setting: 0

Standard Setting: Depends on number of CV steps the user requires.

2.3.9 Address: 16 Read/Write

Size: 16 bit unsigned

Function: Static Bias Control Voltage 1 (representing –50 to +50V DC)

Range: 0 – 65535

Default setting: 0 (-50V)

Format: 1.5259mV per LSB

Standard Setting: 2687 (-45.9V)

2.3.10 Address: 17 Read/Write

Size: 16 bit unsigned

Function: Static Bias Control Voltage 2 (representing –50 to +50V DC)
Range: 0 – 65535
Default setting: 0 (-50V)
Format: 1.5259mV per LSB
Standard Setting: 62848 (+45.9V)

2.3.11 Address: 18 Read/Write
Size: 16 bit unsigned
Function: Static Bias Control Voltage 3 (representing –50 to +50V DC)
Range: 0 – 65535
Default setting: 0 (-50V)
Format: 1.5259mV per LSB
Standard Setting: 2687 (-45.9V)

2.3.12 Address: 19 Read/Write
Size: 16 bit unsigned
Function: Static Bias Control Voltage 4 (representing –50 to +50V DC)
Range: 0 – 65535
Default setting: 0 (-50V)
Format: 1.5412mV per LSB
Standard Setting: 62848 (+45.9V)

2.3.13 Address: 26 Read/Write
Size: 8 bit unsigned
Function: Sets dispersion field pulse width
Range: 0 – 255
Default setting: 0 (off)
Format: 1 LSB = 5ns
Standard Setting: 3 (Corresponding to 15ns)

2.3.14 Address: 27 Read/Write
Size: 8 bit unsigned
Function: Sets dispersion field pulse period
Range: 0 – 255
Default setting: 0 (off)
Format: 1 LSB = 5ns
Standard Setting: 7 (Corresponding to a 35ns period or 28.57 MHz)

2.3.15 Address: 28 Read/Write
Size: 16 bit signed

Function:	Sets ion detector bias voltage 2 (positive)
Range:	-32768 – 32767 (representing -50V to +50V)
Default setting:	0 (0V)
Format:	1.5259mV per LSB
Standard Setting:	-19660 (-30V DC)

2.3.16 Address: 29 Read/Write

Size:	16 bit signed
Function:	Sets ion detector bias voltage 2 (negative)
Range:	-32768 – 32767 (representing -50V to +50V)
Default setting:	0 (0V)
Format:	1.5259mV per LSB
Standard Setting:	19660 (+30V DC)

2.3.17 Address: 30 Read/Write

Size:	8 bit unsigned
Function:	Compensation Voltage step time
Range:	8 - 65535
Default setting:	0
Format:	1 LSB = 212µs
Standard Setting:	15. This register should not be set to values below 8.

2.3.18 Address: 31 Read/Write

Size:	16 bit unsigned
Function:	Sets the dispersion field pulse height 2
Range:	0 – 65535 (representing 0 to ~100.823% Full Scale Dispersion Field)
Default setting:	0
Format:	$1.538461538 \times 10^{-3}$ % full scale per LSB
Standard Setting:	(Varied step-wise in SW to build up dispersion field sweep data)

2.3.19 Address: 44 Read/Write

Size:	16 bit unsigned
Function:	Sets the Compensation Voltage step size fractional part
Range:	0 – 65535
Default setting:	0
Format:	0.000046567mV step size per LSB (additional to the whole part)
Standard Setting:	Depends on whole part and user required step size

Note: Compensation voltage step size whole part and fractional part can be determined from the following formulas:

step size whole part = quotient((step size, mV), (3.0517578125mV))

step size fractional part = round(remainder((step size, mV), (3.0517578125mV))*65536)

Note: the Dispersion field is non-linear above 100% full scale, hence the truncation to approximately 100.823%. The Dispersion Field setting should not exceed 100% Full Scale, *i.e.* the setting sent to registers 10 and 31 should not exceed 65000.

Registers 16, 17, 18 & 19 must be set to the stated +/- 45.9V for proper operation of the Sensor Sub-System.

2.4 Worked command sequence

The sequence of events the local PC shall handle to communicate with the FPGA via the embedded processor can be summarized thus:

Open local communications port

Set Sensor Sub-System control parameters on FPGA (write necessary command strings to FPGA registers, *e.g.* see command sequence below)

Run CV Sweep

Request acquired data message

d<CR>

Re-set pulse amplitude or other FPGA control parameters? If true return to step 2 and re-write to registers as necessary. If false return to step 3 (loop "g" and "d" command).

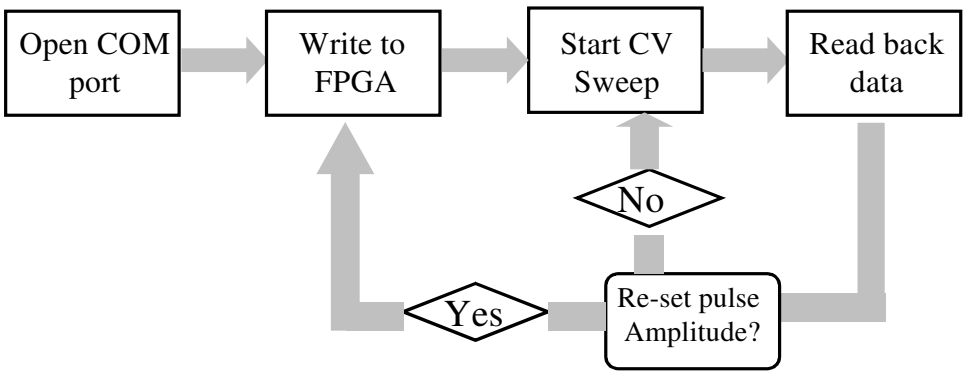

Figure 1: Sequence of operation in Sensor Sub-System.

Note: the start command is simply the ASCII string g followed by a carriage return (*i.e.* g<CR>). Looping the g command would therefore be equivalent to running Sensor Sub-System in "Process Monitoring" mode on LoneStar, while looping with a re-write to registers 10 and 31 would be equivalent to running Sensor Sub-System in "Lab User" mode

Below is a worked example for an ASCII command sequence for operating the Sensor Sub-System. The following command strings would set Sensor Sub-System to perform a Compensation Voltage sweep and read back the subsequent acquired data.

Command String	**Action**
w,2,800<CR>	Sets sensor temperature to 50℃
w,10,32500<CR>	Prepares FPGA to set Dispersion Field pulse height 1 to 50% full scale
w,31,32500<CR>	Prepares FPGA to set Dispersion Field pulse height 2 to 50% full

Command String	Action
	scale
w,13,-2621<CR>	Prepares FPGA to set CV start sweep voltage to –8V
w,14,7 <CR>	Prepares FPGA to set CV sweep step size whole part to 21.36230468 mV
w,44,44557 <CR>	Prepares FPGA to set CV sweep step size fractional part to 2.074885819 mV
w,15,683 <CR>	Prepares FPGA to set number of steps in CV sweep voltage to 683 steps
w,16,2687<CR>	Prepares FPGA to set static bias voltage 1 to –45.9V
w,17,62848<CR>	Prepares FPGA to set static bias voltage 2 to +45.9V
w,19,2687<CR>	Prepares FPGA to set static bias voltage 3 to -45.9V
w,18,62848<CR>	Prepares FPGA to set static bias voltage 4 to +45.9V
w,26,3<CR>	Prepares FPGA to set Dispersion Field pulse width to 15ns
w,27,7<CR>	Prepares FPGA to set Dispersion Field pulse period to35ns (28.57 MHz).
w,28,-19661<CR>	Prepares FPGA to set Ion Detector Bias to –30V
w,29,19661<CR>	Prepares FPGA to set Ion Detector Bias to +30V
w,30,22<CR>	Prepares FPGA to set sample rate to 4.7 ms
	(Software (Labview) controlled RF wait time)
g<CR>	Starts CV sweep
d<CR>	Reads back acquired data (Ion Current data)

Table 1: Example command sequence. **NOTE:** Register settings, 14, 44 and 15

The format of the data that is read back was described in the “Acquired Data String” section (section 4.2). The comma separated values can be translated to a one dimensional array which will have the positive mode CV data in the first half of the array and the negative mode CV data in the second half of the array. The array should be split at an index equal to the number of steps set in register 15. It should be recalled that the CV is swept in the positive and then negative mode by a triangular waveform. The negative mode data array will therefore be reversed to that of the positive mode.

At the end of a scan line all bias amplifiers are reset to zero. Uncalibrated amplifiers will usually exhibit an uncorrected offset of about 1.25V.

2.5 Tips, Caveats and Recommendations for Programming Sensor Sub-System

There are a variety of tips that can be provided to aid the programming of Sensor Sub-System.

2.5.1 CV Oversweep

Under most circumstance one would usually operate with all register settings kept constant with the exception of registers 10 and 31 which are used to alter the DF intensity.

Registers 10 and 31 should always be set to the same value in order to avoid charge build up effects on the FAIMS chip

At the edges of the CV sweep the output voltage is unstable. This creates "glitching" on one edge of the positive mode scan and similar glitching on the other edge of the negative mode scan. To overcome this one must "oversweep" and reject the data on the edges.

Use the 'ok'/'error' return string after writing to registers on the FPGA as an error handler and to create efficiency in your communications.

2.5.2 RF Wait times

It has been shown that running the FAIMS PAD/ Lonestar at 25MHz (26MHz in setup file) can cause excessive heating, based on investigations using a Rev 3.0 Sensor Head board. To run at higher DF levels it is required to pause between scans. It has been shown in previous work that a safe average power the existing FAIMS PAD / Lonestar cooling can cope with is 11W in the MOSFET. To achieve this average power, the off time must be adjusted as function of on time and DF level.

It can be shown that:

$$t_{off} = t_{on}\frac{(1-D)}{D}, \qquad \textbf{Equation 1 Note: if } t_{off} < 0 \textbf{ then } t_{off} = 0$$

where

$$t_{on} = 2\left(N_{steps}\cdot t_{sample} + 2\cdot t_{oversweep}\right),$$

$$D = \frac{P_{\max}}{P_{MOSFET}},$$

$$P_{MOSFET} = a\cdot\exp\left(b\cdot DF\right)$$

and

$$a = 0.3222,\ b = 0.04329,\ P_{\max} = 11\text{W}$$

DF is percentage

Using **Equation 1**, t_{off} was found for a few values of scan time and DF level that previous work had experimentally found a working toff for. The table below compares the measured and calculated values.

Number Steps	DF(%)	Modelled t_{off} (secs)	Measured t_{off} (secs)
512	86	0.54	0.34
512	92	1.45	1.19
1024	84	0.51	0.25
1024	94	3.27	2.78
2048	82	0.17	0.18
2048	94	6.19	5.86

Table 1. Comparison of measured and calculated t_{off} values. t_{sample}=2ms, $t_{oversweep}$=120ms

It can be seen from Table 1 that the calculated t_{off} values are slightly longer than measured. This is no bad thing as it allows a little bit more margin.

Validity of model

- The model has been compared to scan times of 8.67. That is a single line of a DF matrix taking 8.67 seconds (positive and negative mode) to complete. Scan times above this may exceed the maximum MOSFET temperature.

- At very high DF the uncertainty in the measurement of power is huge as it depends on how long the power was applied (due to thermal run-away starting). Therefore, whilst the calculations match measurements pretty well at high DF caution must be used combining long scan times and high DF (>90%).

2.5.3 Heating

The interface board should not be allowed (although it is very unlikely) to overheat. Register 3 should be polled regularly during operation to ensure that overheating is not occurring. The maximum temperature allowed is 90℃. When running the Sensor Sub-System continuously it is recommended that an IF T > 90℃ STOP case is programmed.

2.5.4 Bias voltages

Bias voltages are only applied when the system is sweeping.

2.5.5 Data read

After starting a data read (d) command, data is being sent to the PC as quickly as it is being acquired. Therefore, to reduce delays between compensation voltage sweeps, reading data from the USB port can start immediately after issuing the (d) command. A carriage return <CR> marks the end of the data stream.

Between the (g) command and (d) command, read/write register commands can be sent, e.g. read the sensor temperature and board temperature. This can be done to reduce delay between compensation voltage sweeps.

2.5.6 Propagation delay signal offset

There is a signal propagation delay in the hardware, which causes the positive mode signal to shift to the right and the negative mode signal to the left. This is compensated for by shifting the signals in the opposite direction. Since the signal delay is assumed to be a constant time period, the number of samples to shift the signal by depends on the sampling period.

The formula used for correction is as follows:-

Samples to shift in positive mode = round(4.3 + 4/(sample period,ms + 0.4)

Samples to shift negative = 2 + round(4.3 + 4/(sample period,ms + 0.4)

The positive mode signal is shifted left and the negative mode signal is shifted right.

Since the signal propagation delay depends on hardware components it may be slightly different between units – the difference will be negligible, but it will mean that the Reactant Ion Peak (RIP) is not absolutely offset to zero (with the RF switched off).

2.5.7 Bias amplifier setting

To manually set a bias amplifier read the calibration data from the appropriate register 32 thru 39 and write this to register 42. Write the required DAC value to register 5. Write the amplifier number to bits 12 thru 15 of register 9 together with bit 8.

2.6 Command Summary

The following commands are recognized by the system.

?	Print help text, including the firmware version number.
d	Return ASCII formatted data.

e,reg	Direct read of the contents of EEPROM shadow register.
g	Go, start a scan.
h	Halt, stop scan operation prematurely. This command does not stop the CV ramp. However it will abort further data output.
r,reg	Read an FPGA register
w,reg,value	Write to an FPGA register.

Unrecognised or syntactically incorrect commands generate a message starting with the word error, e.g.

error <CR>

A fuller explanation may follow the word ‘error’ before the carriage return.

3 Appendices

3.1 Appendix 1 – Other registers

This section lists registers that exist in the FPGA but **should not** normally be written by data collection applications.

3.1.1 Address: 5 Read/Write

Size: 16 bit

Function: Diagnostic write data, used in conjunction with register 42 and register 9.

3.1.2 Address: 9 Read/Write

Size: 16 bits wide containing several sub-fields and bits

Function: System control.

Bit	Function	Notes
0	Start sweep	Write as 1 auto clears. Can be read and used as a ramp in progress indicator.
1	Stop sweep	Write as 1 (auto clears?). Does not work
2	System Reset	Write as 1 (auto clears?). Does not work
3	Power Save	Write as 1. Disable 15V and 60V rails. Untested
4	Filter code	Select 1 of 16 sets of filter coefficients. Status unknown/does not work
5		
6		
7		
8	DAC Diag	Write as 1 (auto clears?) to transfer diagnostic registers 5 & 42 to DAC defined by bits 12 to 15
9	ADC Diag	Write as 1 to force continuous conversions, 0 to stop?
10	DF Diag	Write as 1 to force continuous dispersion field, 0 to stop?
11	Reserved	
12	DAC Channel	0000 Positive Bias B (CV) 0001 Negative Bias B (CV) 0010 Positive Bias A (CV) 0011 Negative Bias A (CV) 0100 Static Bias 2 0101 Static Bias 4 0110 Static Bias 3 0111 Static Bias 1 1010 Variable supply (Pulse/DF) 1011...Test Point 418 1xxx Not used
13		
14		
15		

3.1.3 Address: 11 Read/Write

Size: 16 bit signed

Function: Sets ion detector bias voltage 1 (positive)

Range: -32768 – 32767 (representing -50V to +50V)

Default setting: 0 (0V)

Format: 1.5259mV per LSB

Standard Setting: Unused (was for ion pump)

3.1.4 Address: 12 Read/Write

Size: 16 bit signed

Function: Sets ion detector bias voltage 1 (negative)

Range: -32768 – 32767 (representing -50V to +50V)

Default setting: 0 (0V)

Format: 1.5259mV per LSB

Standard Setting: Unused (was for ion pump)

3.1.5 Address: 20 Read/Write

Size: 16 bit unsigned

Function: Static Bias Control Voltage 3, +ve ramp (50 to +50V DC)

Range: 0 – 65535

Default setting: 0 (-50V)

Format: 1.5259mV per LSB

Standard Setting: Unused

3.1.6 Address: 21 Read/Write

Size: 16 bit unsigned

Function: Static Bias Control Voltage 3, -ve ramp (–50 to +50V DC)

Range: 0 – 65535

Default setting: 0 (-50V)

Format: 1.5259mV per LSB

Standard Setting: Unused

3.1.7 Address: 22 Read/Write

Size: 16 bit unsigned

Function: Static Bias Control Voltage 4, -ve ramp (–50 to +50V DC)

Range: 0 – 65535

Default setting: 0 (-50V)

Format: 1.5259mV per LSB

Standard Setting: Unused

3.1.8 Address: 23 Read/Write

Size:	16 bit unsigned
Function:	Static Bias Control Voltage 4, -ve ramp (–50 to +50V DC)
Range:	0 – 65535
Default setting:	0 (-50V)
Format:	1.5412mV per LSB
Standard Setting:	Unused

3.1.9 Address: 24 Read/Write

Size:	13 bit unsigned
Function:	Pointer (address) to internal buffer of ADC conversions
Range:	0 – 8191
Default setting:	0
Standard Setting:	Starts at zero, auto increments when the data register (No. 25) is accessed (read).

3.1.10 Address: 25 Read only

Size:	16 bit unsigned
Function:	ADC conversion data for sample pointer indexed by the address register (reg 24).
Range:	0 – 65535
Notes:	Reading this register will auto increment the address register (No. 24).

3.1.11 Addresses: 32 thru 39 Effectively Read Only

Size:	8 + 8 bits
Function:	Calibration information for a DAC. See Appendix 3.2 for register mapping.
Format	MSB slope, LSB offset.
Default setting:	These resisters are loaded with EEPROM resident data at power on.
Notes:	Writing to these registers also changes the EEPROM shadow copy. These registers must only be written by the standard factory calibration utility. Registers 40 and 41 are not used. They are forced to zero at power on.

3.1.12 Addresses: 40 & 41 Effectively Read Only

Size:	8 + 8 bits
Function:	Calibration information for a DAC. See Appendix 3.2 for register mapping.
Format	MSB slope, LSB offset.
Default setting:	These resisters are effectively unused. They are forced to zero at power on. They are not written to the EEPROM.

3.1.13 Address: 42 Read/Write

Size:	16 bit

Function: Calibration information. Data written to this register is applied to the appropriate DAC using values written to register 5 and register 9.

Format MSB slope, LSB offset.

3.1.14 Address: 43 Read only

Size: 13 bit unsigned

Function: Counts A2D conversions, i.e. it points to the next free entry in the internal conversion buffer. This buffer is accessed via registers 24 (address) and 25 (data).

Range: 0 – 8191

Default setting: 0

Notes: This register is forced to zero when the unit is not ramping. Internally registers are read as two byte reads. During ramping it is possible for this register to change while being read so that the MSB byte reflects the pre-update situation and the LSB byte is the post update value. If a ramp has just completed (register 9 bit 0 has transitioned to zero) then code accessing this register should assume it contains twice the number of CV steps (stored in register 15).

3.2 Appendix 2 – FPGA Register Map

Registers are unsigned unless otherwise stated.

Addr	Width	Type	Name	Description
0	16 bit	RO	Version Revision	Version Control
1	12 bit signed	R/W	Temperature Sensor 1	Controlled Environment Temperature Sensor
2	12 bit signed	R/W	Temperature Set point	Target temperature for Controller
3	12 bit signed	R/W	Temperature Sensor 2	On board (ambient) temperature sensor
4	n/a	R/W	Reserved	Reserved
5	16 bit	R/W	Diagnostic Data	Data used during diagnostic routines
6	n/a	n/a	Reserved	Reserved
7	n/a	n/a	Reserved	Reserved
8	n/a	RO	Reserved	Reserved
9	16 bit	R/W	Control	Control register
10	16 bit	R/W	Pulse_Height_1	High Voltage Pulse Height +ve
11	16 bit	R/W	Bias_Offset_1_Pos	Positive Sweep Offset 1 (not used)
12	16 bit	R/W	Bias_Offset_1_Neg	Negative Sweep Offset 1 (not used)
13	16 bit signed	R/W	Bias_Ramp_Start	Bias (CV) Ramp Starting Voltage
14	16 bit	R/W	Bias_Ramp_Inc	Increment size of Bias (CV) Ramp
15	16 bit	R/W	Bias_Ramp_Step_Cnt	Number of Steps in CV Ramp

Addr	Width	Type	Name	Description
16	16 bit	R/W	Bias_Static_1_Pos	Static voltage bias values set before +ve ramp
17	16 bit	R/W	Bias_Static_1_Neg	Static voltage bias values set before -ve ramp
18	16 bit	R/W	Bias_Static_2_Pos	Static voltage bias values set before +ve ramp
19	16 bit	R/W	Bias_Static_2_Neg	Static voltage bias values set before -ve ramp
20	16 bit	R/W	Bias_Static_3_Pos	Static voltage bias values set before +ve ramp
21	16 bit	R/W	Bias_Static_3_Neg	Static voltage bias values set before -ve ramp
22	16 bit	R/W	Bias_Static_4_Pos	Static voltage bias values set before +ve ramp
23	16 bit	R/W	Bias_Static_4_Neg	Static voltage bias values set before -ve ramp
24	16 bit	R/W	Address_Pointer	Address Pointer to Acquired Data Value
25	16 bit	RO	Data_Register	Register used to read each data point (A2D conversion result)
26	8 bit	R/W	Pulse_Width	High Voltage Pulse Width
27	8 bit	R/W	Pulse_Period	High Voltage Pulse Period
28	16 bit signed	R/W	Bias_Offset_2_Pos	Positive Sweep Offset 2
29	16 bit signed	R/W	Bias_Offset_2_Neg	Negative Sweep Offset 2
30	8 bit	R/W	Sample_Period	Time between samples
31	16 bit	R/W	Pulse_Height_2	High Voltage Pulse Height -ve
32	8+8 bit	R/W	Stat_1_Cal	DAC calibration data - scale (MSB) and offset (LSB)
33	8+8 bit	R/W	Stat_2_Cal	DAC calibration data - scale (MSB) and offset (LSB)
34	8+8 bit	R/W	Stat_3_Cal	DAC calibration data - scale (MSB) and offset (LSB)
35	8+8 bit	R/W	Stat_4_Cal	DAC calibration data - scale (MSB) and offset (LSB)
36	8+8 bit	R/W	Bias_A_Pos_Cal	DAC calibration data - scale (MSB) and offset (LSB)
37	8+8 bit	R/W	Bias_A_Neg_Cal	DAC calibration data - scale (MSB) and offset (LSB)
38	8+8 bit	R/W	Bias_B_Pos_Cal	DAC calibration data - scale (MSB) and offset (LSB)

Addr	Width	Type	Name	Description
39	8+8 bit	R/W	Bias_B_Neg_Cal	DAC calibration data - scale (MSB) and offset (LSB)
40	8+8 bit	R/W	Pulse_Pos_Cal	DAC calibration data - scale (MSB) and offset (LSB). Not used
41	8+8 bit	R/W	Pulse_Neg_Cal	DAC calibration data - scale (MSB) and offset (LSB). Not used
42	8+8 bit	R/W	Diag_Reg_Cal	DAC calibration data - scale (MSB) and offset (LSB). Used with the value in register 5 and applied to the DAC specified by bits in register 9.
43	16 bit	RO	Write Buffer Pointer	Counts A2D conversions as they occur
44	16 bit	R/W	Bias_Ramp_Frac_Inc	Fractional Increment size of Bias Ramp
45 to 63	n/a	n/a	Reserved	Reserved

3.3 Appendix 3 – Windows 7 Driver Installation

- Connect the sensor sub-system to a USB port.
- Navigate to device manager via the control panel.
- A device called ‘Owlstone FAIMS Unit’ should be listed under ‘Other Devices’.
- Select this device and right click. Choose the ‘Update Driver Software’ option.
- In the next window select the option ‘Browse my computer for driver software’.
- On the next window select the ‘Browse’ button and navigate to folder containing the files Mchpcdc.inf and Mchpcdc.cat, then click ‘OK’.
- If a windows security warning is produced select ‘Install this driver anyway’.

Note: the installation appears to take an unexpectedly long time.

- There is a final confirmation that must be dismissed using the ‘Close’ button.

The sensor sub-system will now appear under the ‘Ports (COM & LPT)’ heading with the title ‘Owlstone USB Communications Port’.